



RAN - 1903000203020092



RAN-1903000203020092

S. Y. B. Sc. (Electronics) (Sem. - III) Examination

March - 2023

Electronics : Paper - IV

Advance Digital Electronics and Circuits Design

[Total Marks: 50

સૂચના : / Instructions

(1)

નીચે દર્શાવેલ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fill up strictly the details of signs on your answer book

Name of the Examination:

S. Y. B. Sc. (Electronics) (Sem. - III)

Name of the Subject :

Electronics : Paper - IV Advance Digital Electronics and Circuits Design

Subject Code No.: **1903000203020092**

Seat No.:

| | | | | | |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| <input type="text"/> | <input type="text"/> | <input type="text"/> | <input type="text"/> | <input type="text"/> | <input type="text"/> |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|

Student's Signature

- (2) Figure on the right indicates full marks
- (3) All symbols and abbreviations have their usual meaning.
- (4) Non-programmable calculators are allowed.
- (5) Assume data if necessary.

***O.M.R. Sheet ભરવા અંગેની અગત્યની સૂચનાઓ આપેલ
O.M.R. Sheetની પાછળ છાપેલ છે.***

***Important instructions to fillup O.M.R. Sheet
are given on back side of the provided O.M.R. Sheet.***

1. The advantage of a J-K flip-flop over an S-R FF is that _____.
 - a) It has fewer gates
 - b) It has only one output
 - c) It has no invalid states
 - d) It does not require a clock input

2. Which of the following combinations cannot be combined into K-map group?
 - a) Corners in the same row
 - b) Corners in the same column
 - c) Diagonal
 - d) Overlapping combinations

3. When both inputs of SR latches are low, the latch _____.
 - a) Q output goes high
 - b) Q' output goes high
 - c) It remains in its previously set or reset state
 - d) It goes to its next set or reset state

4. A negative edge-triggered flip-flop will accept inputs only when the clock _____.
 - a) Is LOW
 - b) Changes from HIGH to LOW
 - c) Is HIGH
 - d) Changes from LOW to HIGH

5. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.
 - a) SET
 - b) RESET
 - c) Clear
 - d) Invalid

6. Which of the following is correct for a gated D flip-flop?
 - a) The output toggles if one of the inputs is held HIGH.
 - b) Only one of the inputs can be HIGH at a time.
 - c) The output complement follows the input when enabled.
 - d) Q output follows the input D when the enable is HIGH.

SPACE FOR ROUGH WORK